

## **Innovative Technology Elements for Large and Small Pixel CIS Devices**

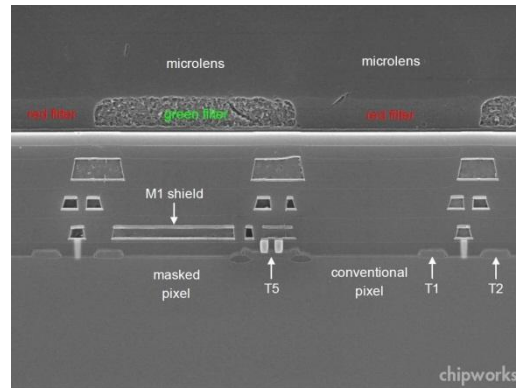
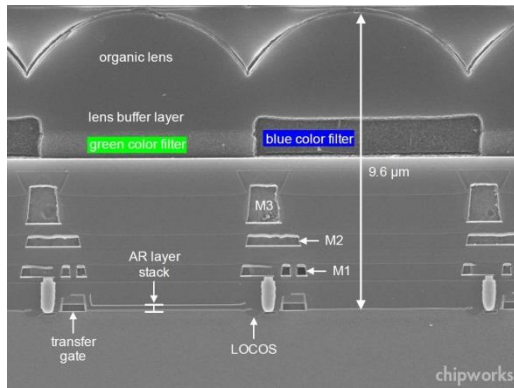
Ray Fontaine  
Technology Analysis Group, Chipworks, Inc.  
1891 Robertson Road, Suite 500  
Ottawa, ON K2H 5B7, Canada  
Email: [rfontaine@chipworks.com](mailto:rfontaine@chipworks.com)  
Voice: (613) 829-0414

The popularity of smartphone cameras has challenged digital compact and interchangeable lens camera manufacturers to differentiate by developing novel pixel structures and innovative chip designs. Impressive video capture capabilities, high-speed on-chip autofocus (AF) systems, and improved low-light performance have resulted in new camera product segments that are perceived to be superior to the state-of-the-art of mobile imaging platforms. Small-pixel mobile imaging devices themselves are rapidly evolving. Pixel shrink continues with 1.1  $\mu\text{m}$  pixels in production and sub-micron pixels in development. Back-illuminated (BI) devices are dominating the primary camera sockets of high-profile smartphones and have also started winning out in secondary camera module sockets. Nevertheless, front-illuminated (FI) device manufacturers continue to innovate and remain competitive to some degree. Chipworks, as a leading supplier of competitive technical analysis to the semiconductor and electronics industries, monitors highly innovative camera systems and image sensor devices as they come in to production.

For the purposes of this paper, large pixel devices are defined as having a  $>4\ \mu\text{m}$  pixel pitch for applications in full-frame (FF) and APS-C format cameras. FF sensors have historically used standalone 4T pixels with a 6  $\mu\text{m}$  to 9  $\mu\text{m}$  pixel pitch. The recent Nikon D800 36 Mp DSLR has pushed its pixel pitch down to 4.75  $\mu\text{m}$  in part due to using pixel sharing, an emerging trend for FF sensors. The manufacturing trend for FF devices is to move off the mature 0.35  $\mu\text{m}$  and 0.25  $\mu\text{m}$  technology generations down to 0.18  $\mu\text{m}$  design rules for Sony and 0.11  $\mu\text{m}$ /0.09  $\mu\text{m}$  rules for the CMOSIS designed, STMicroelectronics fabricated Leica M device.

Recent FF devices are also starting to use novel pixel architectures. Canon and Nikon released the 1D X and D4 FF DSLRs, respectively, both of which sacrificed fill factor to add transistors serving as floating diffusion (FD) node switches. These switches add the flexibility to perform charge-domain binning for video modes.

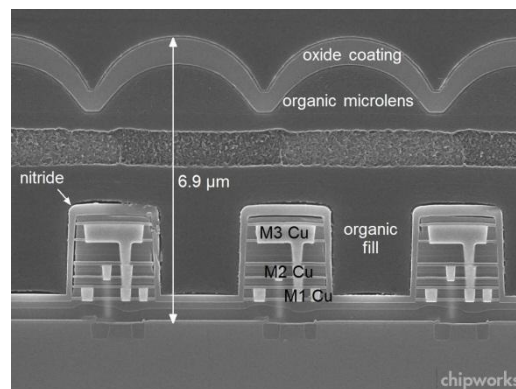
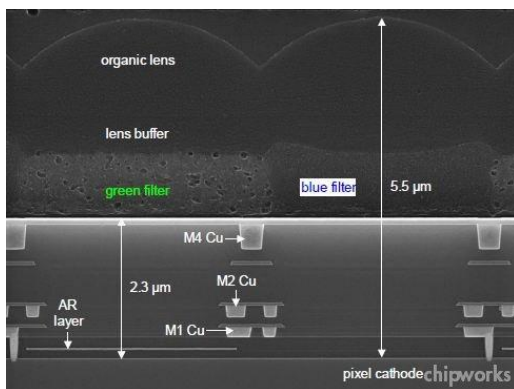
FF pixel structures have evolved through the transfer of legacy small-pixel solutions such as shifting the edge microlenses, color filters, and pixel interconnect towards the array center, and optimizing the metal interconnect patterns for optical symmetry. Nikon has recently engineered color channel dependent pixel anti-reflective (AR) layers. Sony has perhaps the most interesting advancement in FF device production with the release of its SLT-A99 FF interchangeable lens camera. For the first time in a FF sensor, phase detection pixel pairs have been incorporated within rows of active pixels. These on-chip phase detection pixels use a partial pixel mask and are incorporated only within green pixels. Multiple metal 1 mask patterns are used within the phase detection pixel rows, which extend across the entire width of the active pixel array.



**Nikon D4 AR Layers (l), Sony α99 Phase-Detection Pixel (r)**

APS-C format pixel structures have traditionally been comparable to FF pixels, however increasing camera resolutions are forcing pixel sizes down to  $3.9\ \mu\text{m}$  for recent Sony and Toshiba devices. The APS-C pixel shrink enablers can largely be attributed to technology transfers from the domain of small-pixel mobile devices of the recent past. Thinned pixel dielectric stacks, narrow/thin copper BEOL interconnect lines, and microlens coatings have been found in recent APS-C devices.

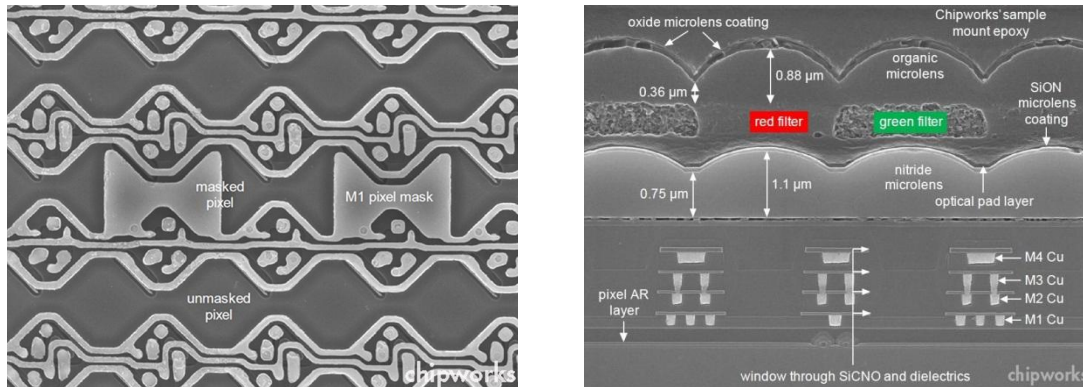
Coinciding with the use of more advanced fabrication technology for APS-C device production, designers now have more flexibility to add functionality to the imaging die. The Toshiba APS-C device from the Nikon D5200 uses 90 nm logic and memory cell libraries, including the first known use of 6T SRAM memory arrays on an APS-C CIS. The BEOL features are aligned with 65 nm design rule metrics, another first for APS-C device production.



**Toshiba (Nikon D5200) Thinned Stack (l), Samsung NX200 Cavity Fill (r)**

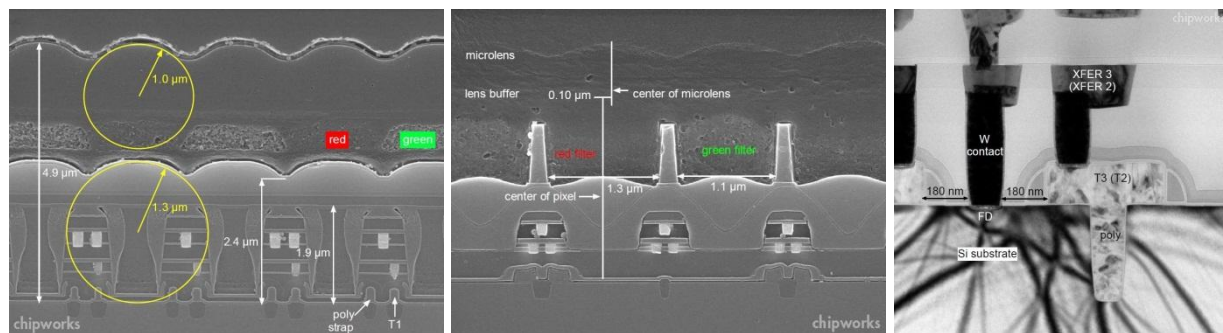
The rise of newer camera formats, such as Nikon's CX (1") format, has resulted in yet another category of imaging devices and associated innovations. This class of cameras generally features a  $2.5\ \mu\text{m}$  to  $4.5\ \mu\text{m}$  pixel size. Recent standouts include Aptina with its dual conversion gain (DCG) pixel architecture for Nikon 1 Series cameras. The DCG pixels feature a double-poly capacitor per shared pixel pair that can boost the capacitance of the FD node in high sensitivity mode. On-chip phase-detection pixels are implemented in nine rows of green pixels extending horizontally nearly the entire width of the active pixel array. The phase detection pixel left and

right half-mask were implemented in the metal 1 interconnect pattern. Sony had a noteworthy 1" format product release with its RX100 sensor. The sensor features an advanced dual microlens scheme and 90 nm Cu BEOL process fully optimized for optical symmetry. The four-shared pixel architecture and clustered transfer gate layout enable a  $2.4\ \mu\text{m}$  pixel pitch and fill factor of about 50%, excluding the microlens contribution.



**Aptina (Nikon V1) Phase Detection Pixels (l), Sony RX100 Dual Microlenses (r)**

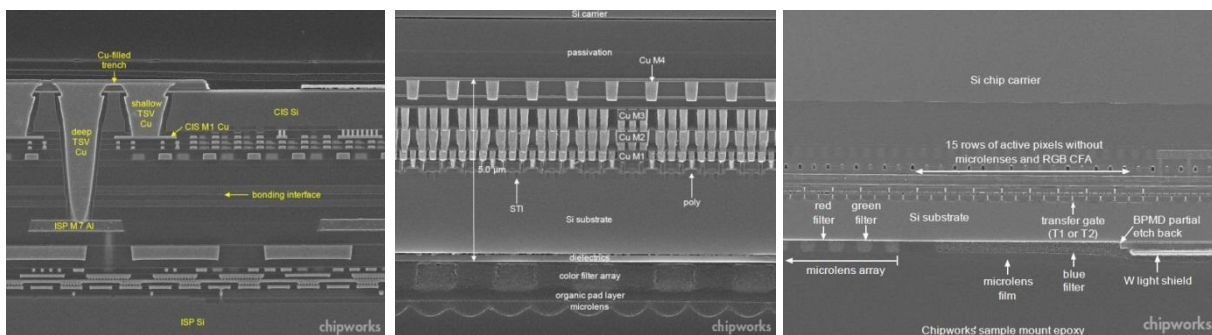
Small pixel devices are classified as having a sub- $2.2\ \mu\text{m}$  pixel pitch and can generally be grouped by end-use. Current digital compact cameras use a mix of front and back-illuminated devices, although BI CIS devices are realizing continued penetration of this application space. Canon used several FI technology elements in its S100 sensor with  $1.85\ \mu\text{m}$  pitch pixels. These include dual microlenses, light pipes, and polysilicon FD strap to facilitate pixel sharing in a thinned dielectric stack. The FI Panasonic device from the DMC-SZ7 features the first known use of 45 nm generation fabrication for an image sensor in its advanced BEOL  $1.4\ \mu\text{m}$  pixels. In addition to narrow interconnect and thin BEOL structures, the device also features depleted channel reset and source follower transistors, and light pipes with embedded color filters. Sony launched its WX100 compact camera with  $1.25\ \mu\text{m}$  pitch BI pixels that employ a unique transfer transistor gate structure comprising a vertical gate region and a planar gate region.



**Canon S100 Light Pipes (l), Panasonic DMC-SZ7 Light Pipes (c), Sony WX100 Vertical Transfer Gate (r)**

The second classification for small pixel devices is reserved for the leading edge of the pixel shrink race generally associated with smartphone and tablet camera modules. OmniVision and Samsung each produced 1.1  $\mu\text{m}$  generation BI devices with anti-reflective layers and optical stacks that evolved from the 1.4  $\mu\text{m}$  generation. Several companies have introduced devices that use RGB + clear color filter patterns. OmniVision in particular plans to couple RGBC with sub-65 nm device production to enable near term small-pixel performance gains [1].

Stacked CIS structures also represent a disruptive technology trend. Sony's stacked CIS camera modules with 1.12  $\mu\text{m}$  pixels entered mass production in 2013 [2]. What was a dummy handle wafer in the BI CIS stack is now an ISP die. Via-last through silicon vias (TSVs) facilitate interconnect between the CIS and ISP dies. Shallow TSVs connecting to the the back of CIS die metal 1 (Cu) landing pads and deep TSVs connecting to the top of ISP metal 7 (Al) pads are connected by a Cu filled trench.



### 1.1 $\mu\text{m}$ Pixel Generation: Sony Stacked CIS (l), OmniVision OmniBSI-2(m), Samsung BI CIS (r)

The reviewed trends show a wide variety of technology elements in use in production devices. This is perhaps unique to the image sensor sector, at least when compared to the high convergence of technology elements in use in logic CMOS or memory sectors. A recent example of continued pixel structure differentiation is the primary CIS from the HTC One smartphone which bucks the megapixel race trend by regressing to a 4.0 Mp resolution with 2.0  $\mu\text{m}$  pixel size for improved low-light performance. The BI CIS, fabricated by STMicroelectronics, was found to have the first use of full-depth, per-pixel deep trench isolation (DTI).

It has been the good fortune of the image sensor industry to have lagged the state-of-the-art of semiconductor device manufacturing by more than a generation. The leading edge is currently represented by Intel's 22 nm logic process. Looking forward, as CIS technologists envision new pixel structures for sub-micron pixel devices it is perhaps inspiring to know the infrastructure is in place to produce the required fine geometry structures.

## References

[1] H. Rhodes, "BSI CMOS Image Sensors with RGBC Technology", IS2013

[2] S. Sukegawa, et al., "A 1/4-inch 8Mpixel Back-Illuminated Stacked CMOS Image Sensor", ISSCC 2013